ABSTRACT

An apparatus and a method for adjusting signal timing in a memory interface have been disclosed. One embodiment of the apparatus includes a number of slave delay lock loops (DLLs) in a memory interface to adjust timing between a number of signals to compensate for timing skew, and a number of input/output (I/O) buffers to output the adjusted signals to one or more memory devices coupled to the memory interface. Other embodiments are described and claimed.